Attorney Docket No.: YOR920040091US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re PATENT APPLICATION of:		
Puneet Gupta et al.		
Appln. No.:	10/787,488	Art Unit:
Filed:	February 26, 2004	Examiner: Unknown
For:	INTEGRATED CIRCUIT LOGIC WITH SELF COMPENSATING BLOCK DELAYS	

SUBMISSION OF FORMAL DRAWINGS

Box PGPUB - DRAWINGS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir,

Enclosed are two (2) sheets of formal drawings including Figures 1 – 3B for publication in the above-identified application.

Respectfully Submitted,

March 23, 2004
(Date)

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I hereby certify that this Correspondence is being deposited with the United States Postal service with sufficient postage for first class mail in an envelope address to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:
Date of Deposit: **March 23, 2004**

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